## REMARKS

The Examiner's Action mailed on August 8, 2003 has been received and its contents carefully considered.

In this Amendment, claim 7 has been amended. Claims 1, 4, 5 and 7 are the independent claims. Claims 1-8 remain pending in the application. For at least the following reasons, it is submitted that this application is in condition for allowance.

Initially, the Examiner is reminded of the telephone conference conducted with Applicant's counsel on August 13, 2003, during which the Examiner agreed that the finality of the office action was premature, due to the new grounds of rejection applied against the subject matter of claim 9, which had been amended into claim 5. The Examiner stated that Applicant should treat this Action as being non-final.

The Examiner has rejected claims 1, 4 and 8 as being anticipated by *Marrs et al.* (USP 5,583,378). It is submitted that these claims are patentably distinguishable over the cited reference for at least the following reasons.

It is well settled that a reference may anticipate a claim within the purview of 35 U.S.C. §102 only if all the features and all the relationships recited in the claim are taught by the reference structure either by clear disclosure or under the principle of inherency.

Applicant's independent claim 1 is directed to a semiconductor device which includes, *inter alia*, a heat spreader having a flat principal surface and having a semiconductor chip and a wiring board provided over the flat principal surface. A common adhesive layer is provided, which is in direct contact with and over the principal surface of the heat spreader and is in direct contact with both the semiconductor chip

and the wiring board so as to bond both the semiconductor chip and the wiring board to the heat spreader, so that a heat transfer effect between the semiconductor chip and the heat spreader is about equal to a heat transfer effect between the wiring board and the heat spreader. Further, claim 1 recites that a portion of the heat spreader within the opening that is not covered by the semiconductor chip is completely covered by the adhesive layer. This claimed configuration reduces any adverse effects, which may be caused by uneven heat transferring, such as warping or inadvertent separation of the various components from the heat spreader. Further advantages are discussed in Applicant's specification, which include preventing concave portions and voids from being formed. This claimed device is not disclosed or suggested by the cited reference.

*Marrs et al.* disclose a ball grid array IC package, which includes a chip 202 that is adhered to a thermal conductor 204 using an adhesive 206. As shown in Figure 2A, adhesive 206 is disposed only over the chip 202, and does not extend beyond the chip.

This reference also discloses using an adhesive layer 210 to adhere thermal conductor 204 to substrate 208. Although not entirely clear, it is believed that this adhesive layer 210 is the feature illustrated in Figure 2A that has the alternating thick, black, diagonal lines, disposed under the oxide layer 228.

Further, this reference teaches that the oxide layer 228 may be formed on the surface of the thermal conductor 204. The oxide layer 228 is used as an adhesion layer to enhance an adhesion between the substrate 208, chip 202, and encapsulating material 226 to the surface 205 of the thermal conductor 204. It is noted that there is no disclosure that this layer 228 has adhesive properties, so that this layer is not disclosed as being an adhesive layer.

This reference also teaches that the surface 205 of the thermal conductor 204 is exposed at a bottom of the well region 236, i.e., the region adjacent to the chip 202, and that the chip 202 is attached directly to the surface 205 using the adhesive 206.

The Examiner's Action has contended that adhesive layers 210 and 206 constitute a common adhesive layer. Although the Examiner's Action appears to acknowledge that these are two separate adhesive layers, the Examiner's Action relies on a case which allegedly stands for the proposition that it is not an invention to provide one layer where the prior art teaches two layers. However, the Examiner's attention is respectfully directed to the fact that the rejection at hand is based on 35 USC Section 102. To the extent that the case relied on by the Action is applicable in rejecting the claims, such rejection could only be based on 35 USC Section 103. That is, under Section 102, a reference may anticipate a claim only if all the features and all the relationships recited in the claim are taught by the reference structure either by clear disclosure or under the principle of inherency. However, the cited reference does not disclose a common adhesive layer which is in direct contact with both the semiconductor chip and the wiring board. Instead, it teaches using two different layers. As such, the cited reference does not anticipate Applicant's claimed invention.

Further, it is noted that the Action states that this case holds that whether one or two of the same identical material is used, does not make the claim patentably distinguishable. However, there is no teaching from the patent that adhesive layers 210 and 206 are identical, as would apparently be required for this case to be applicable.

Further, the Examiner's Action states that adhesive layers 210 and 206 could comprise either one or two layers, since both are adhesives between the chip 202 and

the thermal conductor 204. However, and as discussed above, it is only the adhesive 206 that is between the chip 202 and the thermal conductor 204. The disclosure of this patent makes clear that the adhesive 210 is used only to adhere the thermal conductor 204 to substrate 208, and is not used to adhere the chip to the thermal conductor 204. Otherwise, the adhesive 210 would cover the surface 205 of the thermal conductor 204 in the space between the chip and the substrate. However, this reference instead teaches that the surface 205 in this space is exposed.

Moreover, even if this rejection were based on Section 103, it is noted that the case cited by the Examiner likely does not stand for the broad proposition stated by the Examiner's Action. Moreover, The Federal Circuit has specifically stated that cases that state such *per se* rules should not be applied in rejecting the claims of a patent application. In particular, the court decisions cited in the Action hark back to a time when the presence or absence of "invention" was used as the basic test for patentability, and so-called "negative rules of invention" were developed as an aid to determine when "invention" was present. These negative rules of invention sometimes let to reasonable results but they were also frequently applied in a mechanical way (such as in the present case) to deny patent protection for meritorious inventions. This is one reason why Congress switched away from the "invention" test to the current "non-obviousness" test for patentability. It took awhile for the courts to wean themselves away from the negative rules of invention, but the negative rules are now thoroughly discredited as tests for patentability. Graham v. John Deere, 148 USPQ 459 (S. Ct., 1966) makes it quite clear that non-obviousness, not the presence or absence of "invention," is the basic test for patentability.

Moreover, in its decision in In re Ochia, 37 USPQ2d 1127 (1995), the Court of Appeal for the Federal Circuit stated (at page 1133):

> The use of *per se* rules, while undoubtedly less laborious than a searching comparison of the claimed invention – including all of its limitation – with the teachings of the prior art, flouts section 103, and the fundamental case law applying it. *Per se* rules that eliminate the need for fact-specific analysis of claims and prior art may be administratively convenient for PTO examiners and the Board. Indeed, they have been sanctioned by the Board as well. But reliance on *per se* rules of obviousness is legally incorrect and must cease. Any such administrative convenience is simply inconsistent with section 103, which, according to Graham and its progeny, entitles an applicant to issuance of an otherwise proper patent unless the PTO establishes that the invention *as claimed* in the application is obvious over cited prior art, based on the specific comparison of that prior art with claim limitations. We once again hold today that our precedents do not establish any *per se* rules of obviousness, just at those precedents themselves expressly declined to create such rules. Any conflicts as may be perceived to exist derive from an impermissible effort to extract *per se* rules from decisions that disavow precisely such extraction.

It is respectfully submitted that the position taken by the Examiner's Action, and its reliance on court decisions in an apparent effort to avoid performing a complete search and/or to avoid explaining **why** an ordinarily skilled person would have had an incentive to modify the prior art so as to achieve the present invention, run contrary to the above-quoted guidelines of the CAFC.

Furthermore, the cited reference does not disclose that a heat transfer effect between the chip 202 and the thermal conductor 204 is about equal to a heat transfer effect between the substrate 208 and the thermal conductor, as required by claim 1. In fact, the cited reference makes no comparison between the heat transfer effects of these features at all. Moreover, the Examiner's Action has apparently overlooked this feature, and has failed to address it in the office action.

Moreover, the cited reference does not disclose that a portion of the thermal conductor 204 within the opening that is not covered by the chip is completely covered by a adhesive layer, as recited by claim 1. In fact, this reference teaches away from this claimed feature, since this patent instead teaches that the surface 205 of the thermal conductor 204 is exposed at a bottom of the well region 236, i.e., the region adjacent to the chip 202, and that the chip 202 is attached directly to the surface 205 using the adhesive 206. That is, since this region is exposed, then it is not covered, much less completely covered, by an adhesive layer, as recited in claim 1.

Moreover, Applicant's independent method claim 4 is submitted to be patentably distinguishable over the cited reference for reasons similar to those given above with respect to independent claim 1. It is thus requested that this rejection be withdrawn, and that these claims be allowed.

Further, dependent claim 8 is submitted to be patentably distinguishable over the cited reference for at least the same reasons as independent claim 1, from which this claim depends, as well as for at least the following additional reason.

Claim 8 recites that the common adhesive layer covers the entire principle surface of the heat spreader. In contrast, and as noted above, the cited reference teaches that the surface 205 of the thermal conductor 204 is exposed at a bottom of the well region 236. Thus, the entire principal surface is not covered by an adhesive layer, much less a common adhesive layer. Furthermore, even if this patent disclosed that this portion were covered with an adhesive layer, it is noted that the patent is silent as to the whether the rest of the thermal conductor 204 is covered with an adhesive layer. As such, it is requested that this claim be allowed, and that this rejection be withdrawn.

The Examiner has further rejected claims 2 and 3 as being obvious over *Marrs et al.*, and further in view of *Yamagata et al.* (USP 5,828,127). As noted above, Applicant's independent claim 1 is *prima facie* patentably distinguishable over *Marrs et al.* Moreover, *Yamagata et al.* only disclose providing a fin 19 which is attached utilizing an adhesive 20. This reference does not overcome the above-noted deficiencies of *Marrs et al.*, so that the resulting combination does not disclose or otherwise suggest the features recited within independent claim 1. As such, dependent claims 2 and 3 are submitted to be patentably distinguishable over the cited combination of references for at least the same reasons as independent claim 1, from which these claims depend, as well as for the additional features recited therein. It is requested that these claims be allowed and it is further requested that these rejections be withdrawn.

The Examiner has rejected claims 5 and 6 as being obvious over *Marrs et al.* in view of *Yamagata*, and further in view of *Shin* (USP 5,807,769). It is submitted that these claims are patentably distinguishable over the cited references for at least the following reasons.

Independent claim 5 recites a method which includes connecting electrodes of a semiconductor chip and a wiring board by metal thin wires; sealing a second adhesive layer and part of the semiconductor chip with a first encapsulating resin; and sealing the metal thin wires and the semiconductor chip with a second encapsulating resin after the first encapsulating resin has been cured. Per claim 5, the connecting of the electrodes is performed after sealing the second adhesive layer and part of the semiconductor chip with a first encapsulating resin, and before the sealing of the metal thin wires and the semiconductor chip with a second encapsulating resin. As disclosed by Applicant's

specification, this claimed order of operations prevents voids from occurring, as discussed on page 15, last three lines, through page 16, line 9. This claimed method is neither disclosed nor suggested by the cited references.

As acknowledged by the Examiner's Action, neither *Yamagata* nor *Marrs et al.* teach Applicant's claimed sealing operations. The Action thus relies on the teachings of *Shin* to overcome this admitted deficiency.

*Shin* discloses providing leads 4 around a chip 2, and connecting the leads to a chip using wires 5. After the leads are so connected, a first encapsulating part 6, 6a and a second encapsulating part 7a, 7b are deposited to seal the chip 2, wires 5 and the leads 4.

The Examiner's Action acknowledges that *Shin* does not teach Applicant's claimed order of operations. However, the Action states that the order of steps is irrelevant, and again relies on archaic case law in support for this proposition.

Initially, it is noted that there has never been a case, to the best of Applicant's knowledge, that states that the order of the claimed steps can never lead to the patentably of an invention. Although there may be specific instances where this is true, these instances are limited to where the order of the steps is not deemed to be important or critical to the invention. The Examiner's attention is specifically directed to the MPEP, Section 2144.04, where it is stated that if applicant has demonstrated the criticality of a specific limitation, then it would not be appropriate for the Examiner to rely on case law as the rationale to support the rejection. However, Applicant has demonstrated such criticality, as the specific claimed order of operations is required to reduce voids that may otherwise occur. As such, it is submitted that the Examiner's

Action has failed to establish a *prima facie* case of obviousness against claims 5 and 6, and it is thus requested that these claims be allowed, and that this rejection be withdrawn.

The Examiner has rejected claim 7 as being obvious over *Marrs et al.* in view of *Yamagata*, and further in view of *Shin and Ross* (USP 5,572,070). It is submitted that this claim is patentably distinguishable over the cited references for at least the following reasons.

Claim 7 is directed to a method in which, after electrodes are connected to a wiring board by metal thin wires, a second adhesive layer and part of the semiconductor chip are sealed with an encapsulating resin. After the encapsulating resin has only partially cured, the metal thin wires and the semiconductor chip are sealed with more of the encapsulating resin. The advantages of this method are discussed in Applicant's specification. This claimed method is neither disclosed nor suggested by the cited references.

The Examiner's Action acknowledges that neither *Marrs et al,* nor *Yamagata*, nor *Shin* teach sealing metal thin wires and a semiconductor chip with more encapsulating resin after the first applied resin has partially cured, and relies on the teachings of *Ross* to overcome these admitted deficiencies.

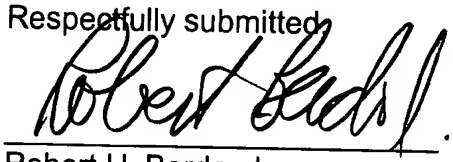
*Ross* teaches a resin layer 20 that is used as a thermal conductive bridge between a die 13 and a lid 17. This reference discloses that a characteristic of this resin includes being in a partially cured state at lower temperatures, and is fully cured at higher temperatures.

However, it is unclear how the Examiner's Action can consider this teaching as overcoming the deficiencies of the other cited references. That is, most, if not all resins go through a semi-cured state prior to being fully cured. Nevertheless, *Ross* does not teach applying more resin after the first resin has partially cured, as recited in claim 7, and thus does not overcome the deficiencies of the other cited references. Moreover, claim 7 now recites that the second applied resin is the same as the first applied resin, and that the second applied resin is cured. If it is the Examiner's contention that the resin of *Ross* is never cured, then this resin could not be used as the second applied resin, as claim 7 requires that this resin be cured. As such, it is submitted that claim 7 is *prima facie* patentably distinguishable over the combination of references relied upon by the Examiner, and it is requested that this claim be allowed. It is further requested that this rejection be withdrawn.

It is submitted that this application is in condition for allowance. Such action and the passing of this case to issue are requested.

Should the Examiner feel that a conference would help to expedite the prosecution of the application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Respectfully submitted,



October 31, 2003
Date

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